II. SPECIFICATION AMENDMENTS

Please amend the paragraph beginning on page 8, line 31 as rewritten below:

The PLL 302 has an input ~~302~~310 for receiving an input clock signal, which input clock signal is the aforementioned master clock signal received over one of the cables 219 from the master sector equipment 110. The input clock signal can be frequency-divided by an input reference clock divider 320 as needed, before transferring it to an input of a phase comparator 330. After the phase comparator 330, the forward path also contains a voltage-controlled oscillator (VCO) 340 as is known in the art, and an output frequency divider 350. The signal F_{out1} 360 represents the slave sector clock signal.